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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,756	07/12/2001	Nobuyuki Hirayama	862.C2290	9593

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EXAMINER	
THOMPSON, JAMES A	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,756	HIRAYAMA, NOBUYUKI	
	Examiner	Art Unit	
	James A. Thompson	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 14 June 2005 have been fully considered but they are not persuasive.

Since all of the original claims 1-9 have been cancelled, all of the rejections and objections listed in the previous office action, dated 15 February 2005, have been withdrawn. Applicant's present arguments are directed to the newly added claims. The rejections to the newly added claims are given in detail below. The new grounds of rejection have been necessitated by the amendments to the claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 10-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (US Patent 5,539,433) in view of Tamura (European Patent Application EP-0811488 A2).

Regarding claims 10, 18, 21 and 22: Kawai discloses a print head assembly (figure 1 of Kawai) comprising an array of printing elements (figure 1(10) and column 3, lines 43-46 of Kawai); a driving circuit (figure 1(50) of Kawai) for selectively driving the printing elements (column 4, lines 35-41

of Kawai); and data supply means (figure 1(5) of Kawai) for supplying driving data to the driving circuit (column 4, lines 45-48 of Kawai), wherein the data supply means comprises a plurality of data supply circuits (figure 2 and column 2, lines 15-16 of Kawai) each arranged to supply data for a corresponding set of the printing elements (column 4, lines 47-56 of Kawai), the data supply circuits being spaced apart in the direction of the array with each data supply circuit being arranged adjacent to the corresponding set of printing elements (figure 2 and column 4, lines 45-52 of Kawai). The plurality of printing elements (figure 1 (10) of Kawai) are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly a single substrate.

Kawai does not disclose expressly that said array of printing elements is divided into a plurality of groups of printing elements; and a selection circuit common to the plurality of groups of printing elements of the array for selecting a printing element to be driven in each group, wherein the selection circuit has common lines coupled to the plurality of groups of printing elements of the array for selecting a printing element to be driven in each group.

Tamura discloses dividing printing elements into a plurality of groups of printing elements (column 5, lines 44-51 of Tamura); and a selection circuit (figure 2(1701-1704) of Tamura) which is common to the plurality of groups of printing elements (column 5, lines 19-20 of Tamura) of the array for selecting a printing element to be driven in each group (column 5, lines 49-51 and column 6, lines 16-20 of Tamura), wherein the selection circuit has common lines coupled to the plurality of groups of printing elements of the array for selecting a

printing element to be driven in each group (figure 2(1705→IJH) and column 5, lines 37-41 of Tamura).

Kawai and Tamura are combinable because they are from the same field of endeavor, namely the digital control of printheads and printhead data. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the plurality of groups and a selection circuit to select a printing element from each group, according to the teachings of Tamura, in the overall printhead taught by Kawai. Since the printhead of Kawai is a single integrated device (figure 1 of Kawai), the selection circuit taught by Tamura would also be arranged on the substrate, said substrate being the substrate that is inherently required to form a physical digital circuit. The motivation for doing so would have been that constant switching of power components creates a large power loss and requires bulky circuits (column 2, lines 44-57 of Tamura) and using a diode or transistor matrix requires a disadvantageous number of wiring lines, which increases cost and degrades reliability (column 2, line 58 to column 3, line 7 of Tamura). Both of these problems are solved by using the selection circuit taught by Tamura (column 3, lines 11-14 of Tamura). Therefore, it would have been obvious to combine Tamura with Kawai to obtain the invention as specified in claims 10, 18, 21 and 22.

Further regarding claim 10: The print head substrate of claim 10 is fully embodied in the print head of claim 18.

Further regarding claim 21: Kawai further discloses an ink tank for storing ink to be supplied to the print head (column 24, lines 58-60 of Kawai).

Further regarding claim 22: Kawai further discloses driving data generation means (figure 1(6) and column 3, lines

36-38 of Kawai) for generating a data signal for each path of the data supply circuits (column 3, lines 38-45 of Kawai). The driving data generation means (figure 1(6) of Kawai) controls the overall apparatus (column 3, lines 36-38 of Kawai), and thus the reading of the temperature data from the ROM and the tonal data from the density counter, which is used to control the driving of the printhead (column 3, lines 38-45 of Kawai).

Regarding claim 11: Kawai discloses that the plurality of print head assemblies are provided on the substrate (figure 2; column 2, lines 15-16; and column 3, lines 29-36 of Kawai). The thermal head (figure 1(10) of Kawai) contains a plurality of print head assemblies since said thermal head prints a plurality of primary colors (column 3, lines 29-36 of Kawai). Said plurality of print head assemblies are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly a single substrate.

Regarding claim 12: Kawai discloses that the data supply circuits (figure 1(5) and column 3, lines 23-25 of Kawai) include a plurality of shift registers (figure 2(17) of Kawai) for receiving clock and data signals (figure 2("DATA","CLOCK") and column 3, lines 53-55 of Kawai), a plurality of latches (figure 2(16) of Kawai) for latching output signals from the shift registers (column 3, lines 50-53 of Kawai), and AND circuits (figure 2($A_1 \ldots A_n$) of Kawai) for deriving a logical product of outputs from the latches and a driving signal (column 3, lines 55-62 of Kawai). The latch circuit (figure 1(16) of Kawai) comprises multiple latches (column 4, lines 48-51 of Kawai "latched in the latches 16, at the same time supplied to the AND gates"). Further, Kawai teaches in another embodiment using multiple shift registers (figure 20(117a-117c) of Kawai)

for multiple data and clock signals to supply the necessary signals to the selected heating elements (figure 20(115) of Kawai) which are energized based on multiple strobe signals (figure 20(119a-119c) and column 18, line 63 to column 19, line 4 of Kawai). The use of multiple shift registers would be obvious to one of ordinary skill in the art at the time of the invention, especially given the combination of Kawai in view of Tamura in which a printing element is driven in each of a plurality of groups of printing elements (column 5, lines 49-51 and column 6, lines 16-20 of Tamura). If there are multiple groups or divisions of printing, such as in Tamura or as shown in figure 20 of Kawai, then one of ordinary skill in the art would use multiple shift registers.

Regarding claim 13: Kawai discloses that there are two data supply circuits (figure 2(A_1,Q_1,R_1) and figure 2(A_n,Q_n,R_n) of Kawai) arranged at respective ends of the printing array elements (figure 2 and column 3, lines 55-62 of Kawai).

Regarding claims 14-15: Kawai discloses that the array of printing elements extends alongside an ink supply port (figure 27(255); column 3, lines 58-62; and column 24, line 58 to column 25, line 5 of Kawai). An ink supply port (figure 27(255) of Kawai) provides ink to the thermal heating elements (column 24, lines 58-66 of Kawai). Heat is generated to activate each of the printing elements based on the printing data (column 3, lines 58-62 of Kawai), which causes the ink to be heated and properly discharged on the paper (column 24, line 66 to column 25, line 5 of Kawai). Thus, the array of printing elements extends alongside the ink supply port since the array of printing elements provides the heat supplied to the ink supplied by said ink supply port.

Further regarding claim 16: Tamura discloses that said selection circuit (figure 2(1701-1705) of Tamura) is arranged at one end of the printing element array (as shown clearly in figure 2 of Tamura). The selection circuit is connected to the printing element array, which is located in the recording head (figure 2(IJH) of Tamura).

Regarding claim 17: Kawai discloses that said substrate is rectangular (figure 27(250) and column 24, lines 50-58 of Kawai) and the printing elements array extends along the length of the rectangle (figure 27(251) and column 24, lines 52-53 of Kawai). As can clearly be seen in figure 27 of Kawai, the substrate is rectangular and the printing elements array (figure 27(251) of Kawai) extends along the length of said rectangle.

Regarding claim 19: Kawai discloses that the print head is an ink jet head (figure 27(202) of Kawai) for printing data by discharging ink (column 24, lines 50-52 and lines 58-61 of Kawai).

Regarding claim 20: Kawai discloses that the print head comprises electrothermal transducing means (figure 2(15) of Kawai) for generating thermal energy to cause ink discharge (column 4, lines 50-55 of Kawai).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Thompson whose telephone number is 571-272-7441. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Thompson
Examiner
Art Unit 2624

JAT
15 August 2005

THOMAS D. ~~TOMMY~~ LEE
PRIMARY EXAMINER